The following list of claims replace the previous claims.

Claim 1 (previously presented): A method of manufacturing an electronic device comprising thin-film circuit elements that include a diode integrated with a crystalline thin-film transistor, the transistor having a channel area in an active semiconductor film that is more crystalline than an active semiconductor film of the diode, comprising:

forming on a circuit substrate the crystalline active semiconductor film of the transistor with a first process involving a first processing temperature;

forming doped source and drain regions of the transistor at ends of the channel area with a second process involving a second processing temperature;

providing an interconnection film between an electrode area of the transistor and a diode area over which the diode is to be formed, and providing an etch-stop film on which the active semiconductor film for the diode is to be deposited;

depositing the active semiconductor film for the diode over the interconnection film and the etch-stop film with a third process that involves a third processing temperature, the first and second processing temperatures being higher than the third processing temperature; and

etching away the active semiconductor film for the diode from over the etch-stop film to leave the active semiconductor film for the diode over the interconnection film in the diode area;

wherein the diode has its active semiconductor film forming an intrinsic region between P and N electrode regions of a vertical PIN diode structure, and wherein the interconnection film comprises a doped region in a semiconductor film together with the doped source and drain

regions of the transistor and a bottom one of the P and N electrode regions of the PIN diode.

Claim 2 (previously presented): The method of claim 1, wherein the etch-stop film is an insulating film that extends over the interconnection film and that has a window at the diode area to permit contact between the interconnection film and the active semiconductor film of the diode.

Claim 3 canceled.

Claim 4 (previously presneted): The method of claim 1, wherein regions of the crystalline active semiconductor film are doped to provide the source and drain regions of the transistor, the bottom one of the P and N electrode regions of the PIN diode, and the interconnection film therebetween.

Claim 5 (previously presneted): The method of claim 1, wherein at least a portion of the interconnection film is provided on a gate-dielectric film on the crystalline active semiconductor film to form a doped-semiconductor top gate electrode of the transistor which is interconnected with the bottom one of the P and N electrode regions of the PIN diode.

Claim 6 (previously presented): The method of claim 5, wherein the PIN diode is formed on the gate-dielectric film on the crystalline active semiconductor film of the transistor.

Claim 7 (previously presented): The method of claim 4, wherein the electronic device comprises first and second crystalline thin-film transistors integrated with the PIN diode by the interconnection film, and wherein the interconnection

film provides the bottom one of the P and N electrode regions of the PIN diode, the top gate electrode of the first transistor, and/or the source and drain regions of the second transistor.

Claim 8 (previously presented): The method of claim 1, wherein the interconnection film comprises metal which provides the etch-stop film, and the diode has a vertical PIN diode structure formed in its active semiconductor film as an intrinsic region between P and N electrode regions.

Claim 9 (currently amended): A method of manufacturing an electronic device comprising thin-film circuit elements that include a diode integrated with a crystalline thin film transistor, the transistor having a channel area in an active semiconductor film that is more crystalline than an active semiconductor film of the diode, comprising:

forming on a circuit substrate the crystalline active semiconductor film of the transistor with a first process involving a first processing temperature;

forming doped source and drain regions of the transistor at ends of the channel area with a second process involving a second processing temperature;

providing an interconnection film between an electrode area of the transistor and a diode area over which the diode is to be formed, and providing an etch-stop film on which the active semiconductor film for the diode is to be deposited;

depositing the active semiconductor film for the diode over the interconnection film and the etch-stop film with a third process that involves a third processing temperature, the first and second processing temperatures being higher than the third processing temperature; and

etching away the active semiconductor film for the diode from over the etch-stop film to leave the active semiconductor film for the diode over the interconnection film in the diode area;

wherein at least a portion of the ~~etch-stop~~ interconnection film is provided on a gate-dielectric film on the crystalline active semiconductor film to form a top gate electrode of the transistor which is interconnected with a bottom one of the P and N electrode regions of the PIN diode.

Claim 10 (previously presented): The method of claim 9, wherein the PIN diode is formed on the gate-dielectric film on the crystalline active semiconductor film of the transistor.

Claim 11 (previously presented): The method of claim 9, wherein the electronic device comprises first and second crystalline thin-film transistors integrated with the PIN diode by the interconnection film, and wherein the interconnection film connects the bottom one of the P and N electrode regions of the PIN diode, the top gate electrode of the first transistor, and the source region of the second transistor.

Claim 12 (previously presented): The method of claim 7, wherein the electronic device comprises an active-matrix electroluminescent display with a light-emitting diode in each pixel, and wherein the light-emitting diode is driven via the first transistor as addressed via the second transistor.

Claim 13 (previously presented): The method of claim 1, wherein the crystalline semiconductor film is subjected to a hydrogenation process.

Claim 14 (previously presented): The method of claim 1, wherein the crystalline semiconductor film is formed by crystallising a deposited semiconductor film using laser heating of the film.

Claim 15 (previously presented): The method of claim 1, wherein the doped source and drain regions are formed by an ion implant of dopant in the crystalline semiconductor film and by annealing the implanted dopant.

Claims 16-18 (Canceled).

Claim 19 (previously presented): The method of claim 5, wherein the electronic device comprises first and second crystalline thin-film transistors integrated with the PIN diode by the interconnection film, and wherein the interconnection film provides the bottom one of the P and N electrode regions of the PIN diode, the top gate electrode of the first transistor, and/or the source and drain regions of the second transistor.

Claim 20 (previously presented): The method of claim 10, wherein the electronic device comprises first and second crystalline thin-film transistors integrated with the PIN diode by the interconnection film, and wherein the interconnection film connects the bottom one of the P and N electrode regions of the PIN diode, the top gate electrode of the first transistor, and the source region of the second transistor.

Claim 21 (previously presented): The method of claim 11, wherein the electronic device comprises an active-matrix

electroluminescent display with a light-emitting diode in each pixel, and wherein the light-emitting diode is driven via the first transistor as addressed via the second transistor.